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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/666,228	09/18/2003	Franz Hirler	MUH-12747 C	8480

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EXAMINER	
PERALTA, GINETTE	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 10/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/666,228	HIRLER ET AL.	
	Examiner	Art Unit	
	Ginette Peralta	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,5 and 6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,5,and 6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/392,024.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 3, 5, and 6 are rejected under 35 U.S.C. 102(e) as being anticipated by Lanzerstorfer et al. (U. S. Pat. 6,605,841 B2).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Regarding claim 1, Lanzerstorfer et al. discloses in fig. 2H a power transistor having at least one trench transistor cell in a semiconductor body comprising a drain zone *12*, a drift zone *122*, a channel zone *14*, and a source zone *70* formed in each case successively and substantially horizontally in the semiconductor body *(col. 7, lines 34-53, and col. 10, lines 7-23)*; the semiconductor body having a trench *22A* formed therein

with a base and a defined body height opposite a pn junction between the drift zone *122* and the channel zone *14*; a first dielectric layer *120A* cladding the trench *22A* substantially to the body height, and a gate oxide *34A* cladding the trench *22A* between the body zone and a semiconductor body surface; and a field electrode *40A* extending in the trench *22A* substantially from the trench base to an upper edge of the first dielectric layer *120A*, the field electrode *40A* being connected to be at a fixed potential disclosed in col. 10, lines 35-40 or at a source potential along with the gate electrode as shown in Fig. 6 as connected to the source potential *S1* and as taught in col. 6, lines 49-53; a gate electrode *60A* disposed substantially between the body height and the semiconductor body surface, the gate electrode *60A* being electrically insulated from the semiconductor body by the gate oxide *34A* and having a lower edge with a profile, the profile being at least partly obliquely angled relative to the semiconductor body; and a second dielectric layer *50A* formed between the gate electrode *60A* and the field electrode *40A*.

Regarding claim 3, Lanzerstorfer et al. discloses in Fig. 6 that the profile has a falling angle between two trenches.

Regarding claim 5, Lanzerstorfer et al. discloses in Fig. 6 the field electrode *40A* overlapping the gate electrode *60A*.

Regarding claim 6, Lanzerstorfer et al. discloses in Fig. 6 that the field electrode *40A* intersects and passes through a plane defined by the pn junction between the drift zone *122* and the channel zone *14*.

Response to Arguments

3. Applicant's arguments filed 6/22/05 have been fully considered but they are not persuasive.

Regarding applicant's argument that the profile of the bottom edge of the gate electrode is at least partly obliquely angled relative to the semiconductor body surface and/or has a horseshoe shape wherein two jaws project at edges thereof, and that in contrast Lanzerstorfer et al. discloses that the lower edge of the gate electrode is rounded which cannot be considered as at least partly obliquely angled relative to the semiconductor body surface, it is noted that in a rounded or arched structure all segments are obliquely angled relative to a certain plane, therefore there are portions of the rounded gate electrode of Lanzerstorfer et al., as small as they may be, that are obliquely angled relative to the semiconductor body surface, and thus the claimed feature is anticipated by Lanzerstorfer et al..

Regarding applicant's argument that it can be derived from the claim language that the gate electrode is clearly provided above the filed electrode so that in none of the embodiments is the top surface of the field electrode on the same level as the top surface of the gate electrode as derived from the limitations of claim 1 of " a first dielectric layer cladding said trench substantially to said body height," "a field electrode extending in said trench substantially from said trench base to an upper edge of said first dielectric layer" and a "gate electrode disposed substantially between said body height and the semiconductor body surface" and that Lanzerstorfer et al. discloses

that the field electrode 40A envelopes the gate electrode 60A so that the field electrode 40A reaches the same level as the gate electrode 60A, it is noted that the claim language refers to "a field electrode extending in said trench substantially from said trench base to an upper edge of said first dielectric layer" and since the field electrode extends to *substantially* the *upper edge* of the dielectric layer it goes over the dielectric layer, the claim language teaches that the field electrode goes over the dielectric layer, and it does not preclude that the field electrode and the gate electrode may be at the same level.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ginette Peralta whose telephone number is (571) 272-1713. The examiner can normally be reached on Monday to Friday 8:00 AM- 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

GP

HOA PHAM
PRIMARY EXAMINER